1/18

Fig.1

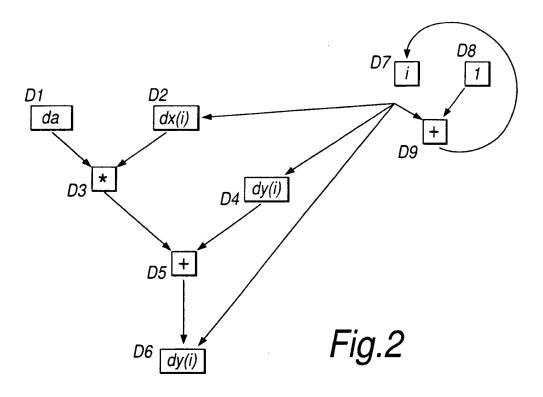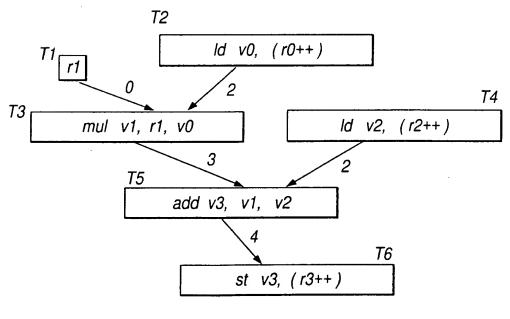## 2/18

Fig.2

Fig.3

PREDICATED EXECUTION OF INSTRUCTIONS . . .
Nigel Peter Topham and Adrian Philip Wise
Greer, Burns & Crain, Ltd. (Patrick Burns)
Ref. No. 0808.65566
Sheet 3 of 18   (312) 360 0080

3/18

Stage	Cycle	Issue slot 1	Issue slot 2	Issue slot 3	v0	v1	v2	v3
1	0	ld v0, (r0++)			s0			
	1				s0			
2	2			mul v1, v0, r1	s1	s2		
	3	ld v2, (r2++)				s2	s4	
3	4					s3	s5	
	5			add v3, v1, v2		s3	s5	s6
4	6							s7
	7							s7
5	8							s8
	9		st v3, (r3++)					s8

Fig.4

4/18

120

Physical register file

120R

register N-1

N-K registers are addressed using an offset which varies between zero and N-K-1.

register K

B

120S

K registers are directly addressed by the logical register number

register 0

Fig.5

PREDICATED EXECUTION OF INSTRUCTIONS
Nigel Peter Topham and Adrian Phili
Greer, Burns & Crain, Ltd. (Patrick   s)
Ref. No. 0808.65566
Sheet 5 of 18   (312) 360 0080

5/18

Cycle	Offset	Iteration 0					Iteration 1				
		Instruction	v0	v1	v2	v3	Instruction	v0	v1	v2	v3
0	6	ld v0, (r0++)	r4 (▸ p10)								
1	6		r4 (▸ p10)								
2	5	mul v1, v0, r1	r5 (▸ p10)	r6 (▸ p11)			ld v0, (r0++)	r4 (▸ p9)			
3	5	ld v2, (r2++)		r6 (▸ p11)	r8 (▸ p13)			r4 (▸ p9)			
4	4			r7 (▸ p11)	r9 (▸ p13)		mul v1, v0, r1	r5 (▸ p9)	r6 (▸ p10)		
5	4	add v3, v1, v2		r7 (▸ p11)	r9 (▸ p13)	r10 (▸ p14)	ld v2, (r2++)		r6 (▸ p10)	r8 (▸ p12)	
6	3					r11 (▸ p14)			r7 (▸ p10)	r9 (▸ p12)	
7	3					r11 (▸ p14)	add v3, v1, v2		r7 (▸ p10)	r9 (▸ p12)	r10 (▸ p13)
8	2					r12 (▸ p14)					r11 (▸ p13)
9	2	st v3, (r3++)				r12 (▸ p14)					r11 (▸ p13)
10	1										r12 (▸ p13)
11	1						st v3, (r3++)				r12 (▸ p13)

Fig.6A

6/18

Cycle	Offset	Iteration 2					Iteration 3				
		Instruction	v0	v1	v2	v3	Instruction	v0	v1	v2	v3
0	6										
1	6										
2	5										
3	5										
4	4	ld v0, (r0++)	r4 (▸ p8)								
5	4		r4 (▸ p8)								
6	3	mul v1, v0, r1	r5 (▸ p8)	r6 (▸ p9)							
7	3	ld v2, (r2++)		r6 (▸ p9)	r8 (▸ p11)		ld v0, (r0 ++)	r4 (▸ p7)			
8	2			r7 (▸ p9)	r9 (▸ p11)			r4 (▸ p7)			
9	2	add v3, v1, v2		r7 (▸ p9)	r9 (▸ p11)	r10 (▸ p12)	mul v1, v0, r1	r5 (▸ p7)	r6 (▸ p8)		
10	1					r11 (▸ p12)	ld v2, (r2++)		r6 (▸ p8)	r8 (▸ p10)	
11	1					r11 (▸ p12)			r7 (▸ p8)	r9 (▸ p10)	
12	0					r12 (▸ p12)	add v3, v1, v2		r7 (▸ p8)	r9 (▸ p10)	r10 (▸ p11)
13	0	st v3, (r3++)				r12 (▸ p12)					r11 (▸ p11)
14	-1										r11 (▸ p11)
15	-1						st v3, (r3++)				r12 (▸ p11)

Fig.6B

7/18

Cycle	Offset	Iteration 0 Instruction	Iteration 1 Instruction	Iteration 2 Instruction	Iteration 3 Instruction
0	6	ld r4, (r0++)			
1	6				
2	5	mul r6, r5, r1	ld r4, (r0++)		
3	5	ld r8, (r2++)			
4	4		mul r6, r5, r1	ld r4, (r0++)	
5	4	add r10, r7, r9	ld r8, (r2++)		
6	3			mul r6, r5, r1	ld r4, (r0++)
7	3		add r10, r7, r9	ld r8, (r2++)	
8	2				mul r6, r5, r1
9	2	st r14, (r3++)		add r10, r7, r9	ld r8, (r2++)
10	1				
11	1		st r12, (r3++)		add r10, r7, r9
12	0				
13	0			st r12, (r3++)	
14	-1				
15	-1				st r12, (r3++)

Fig.7

8/18

Cycle	Offset	Iteration 0 Instruction	Iteration 1 Instruction	Iteration 2 Instruction	Iteration 3 Instruction
0	6	ld p10, (p0++)			
1	6				
2	5	mul p11, p10, p1	ld p9, (p0++)		
3	5	ld p13, (p2++)			
4	4		mul p10, p9, p1	ld p8, (p0++)	
5	4	add p14, p11, p13	ld p12, (p2++)		
6	3			mul p9, p8, p1	ld p7, (p0++)
7	3		add p13, p10, p12	ld p11, (p2++)	
8	2				mul p8, p7, p1
9	2	st p14, (p3++)		add p12, p9, p11	ld p10, (p2++)
10	1				
11	1		st p13, (p3++)		add p11, p8, p10
12	0				
13	0			st p12, (p3++)	
14	-1				
15	-1				st p11, (p3++)

Fig.8

PREDICATED EXECUTION OF INSTRUCTIONS . . . .
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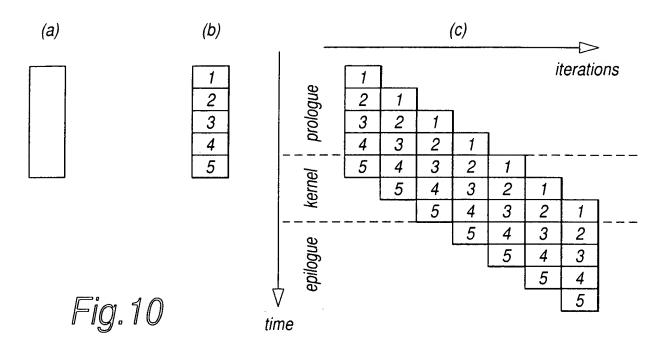Ref. No. 0808.65566
Sheet 9 of 18   (312) 360 0080

9/18

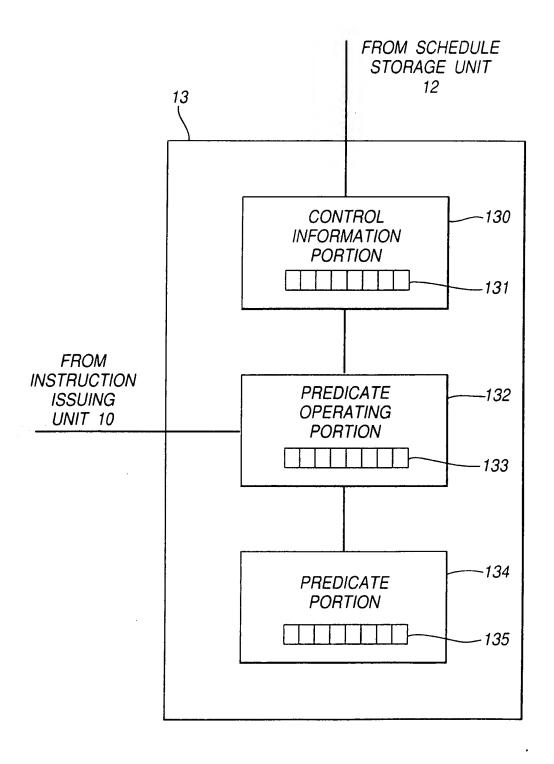| Cycle	Issue slot 1			Issue slot 2			Issue slot 3		
	Instruction	Iteration	Stage	Instruction	Iteration	Stage	Instruction	Iteration	Stage
0	ld r4, (r0++)	0	1						
1									
2	ld r4, (r0++)	1	1				mul r6, r5, r1	0	2
3	ld r8, (r2++)	0	2						
4	ld r4, (r0++)	2	1				mul r6, r5, r1	1	2
5	ld r8, (r2++)	1	2				add r10, r7, r9	0	3
6	ld r4, (r0++)	3	1				mul r6, r5, r1	2	2
7	ld r8, (r2++)	2	2				add r10, r7, r9	1	3
8							mul r6, r5, r1	3	2
9	ld r8, (r2++)	3	2	st r12, (r3++)	0	5	add r10, r7, r9	2	3
10									
11				st r12, (r3++)	1	5	add r10, r7, r9	3	3
12									
13				st r12, (r3++)	2	5			
14									
15				st r12, (r3++)	3	5			

Fig.9

PREDICATED EXECUTION OF INSTRUCTIONS . . .
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Ref. No. 0808.65566
Sheet 10 of 18   (312) 360 0080

10/18

(a)   (b)   (c)

iterations

prologue / kernel / epilogue

time

Fig.10

						P5	P4	P3	P2	P1
1						0	0	0	0	1
2	1					0	0	0	1	1
3	2	1				0	0	1	1	1
4	3	2	1			0	1	1	1	1
5	4	3	2	1		1	1	1	1	1
	5	4	3	2	1	1	1	1	1	1
		5	4	3	2	1	1	1	1	1
			5	4	3	2	1	1	1	1	0
				5	4	3	1	1	1	0	0
					5	4	1	1	0	0	0
						5	1	0	0	0	0

prologue / kernel / epilogue

time

Fig.11

FROM SCHEDULE
STORAGE UNIT
12

13

CONTROL
INFORMATION
PORTION — 130

— 131

FROM
INSTRUCTION
ISSUING
UNIT 10

PREDICATE
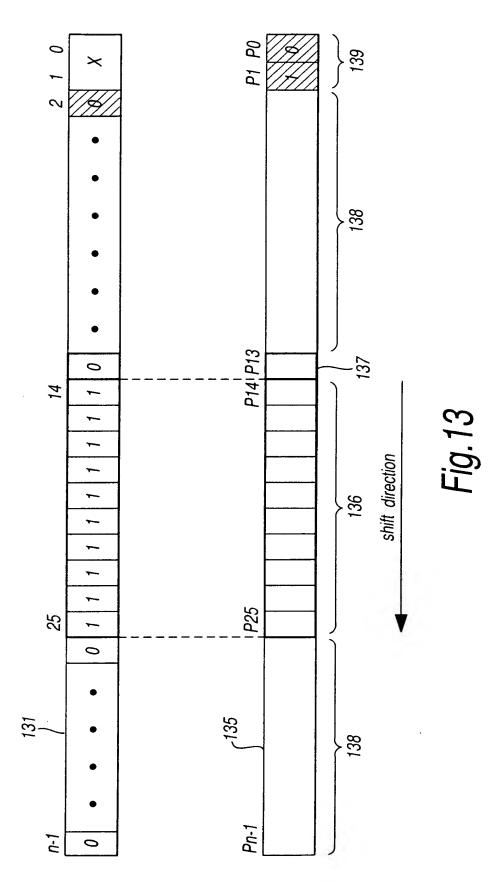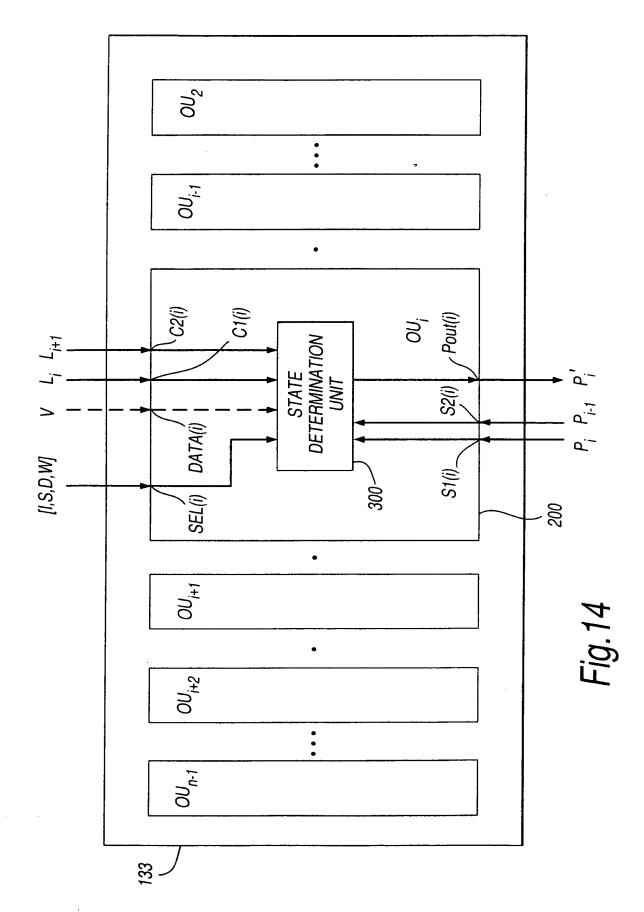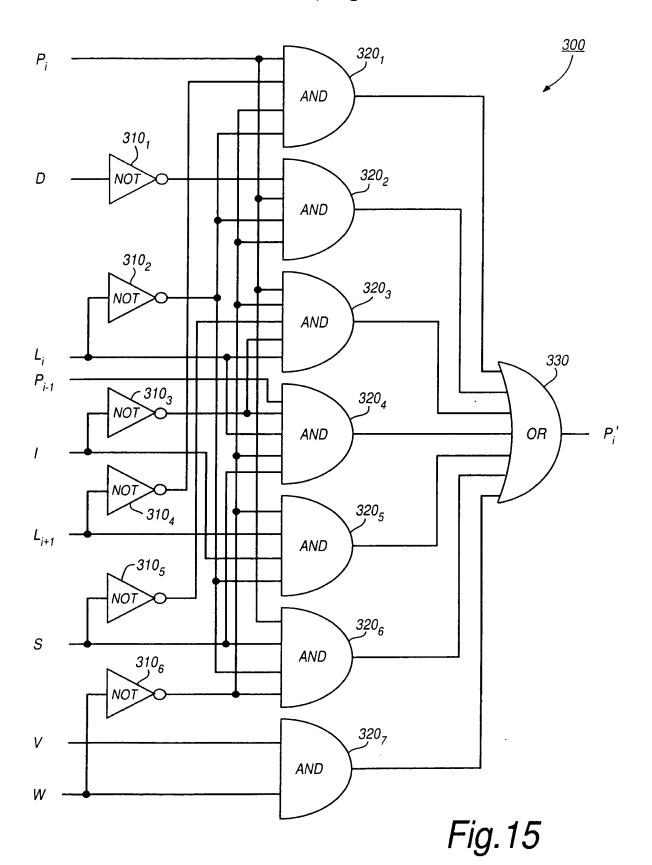OPERATING
PORTION — 132

— 133

PREDICATE
PORTION — 134

— 135

Fig.12

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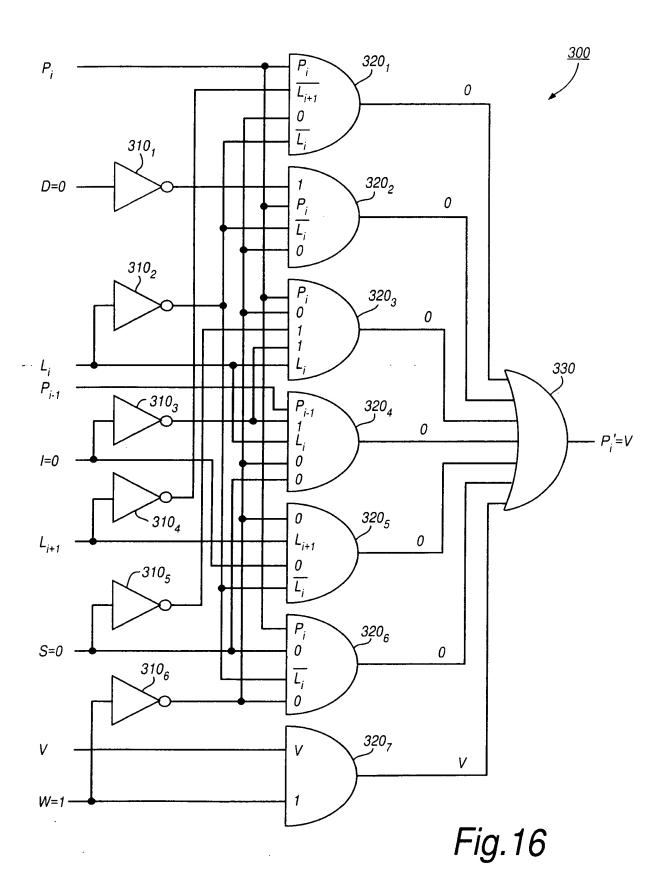Ref. No. 0808.65566
Sheet 12 of 18   (312) 360 0080

12/18

Fig.13

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Ref. No. 0808.65566
Sheet 13 of 18   (312) 360 0080

13/18

Fig.14

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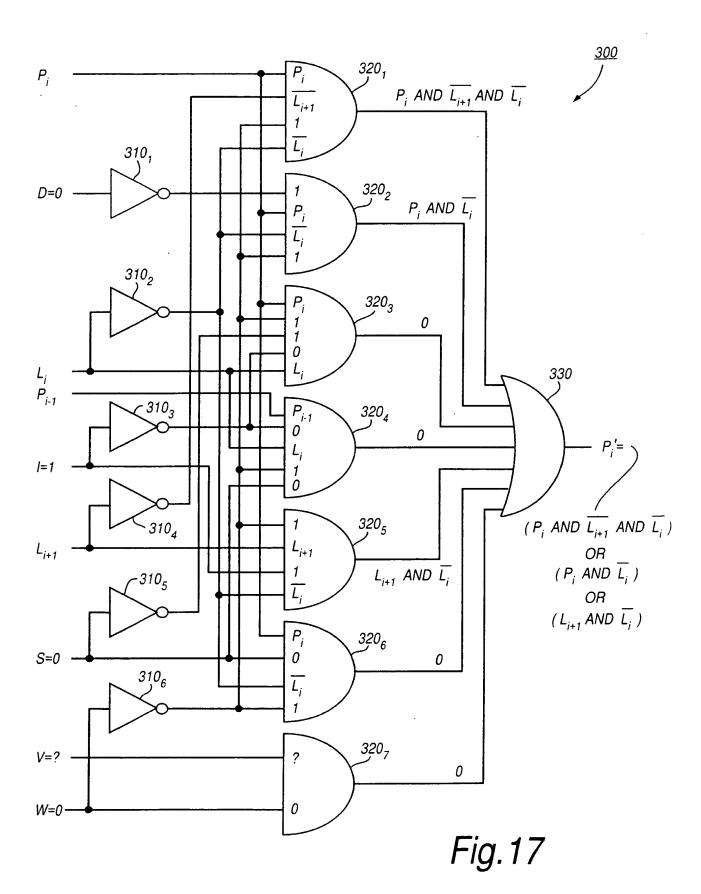Ref. No. 0808.65566
Sheet 14 of 18   (312) 360 0080

14/18

Fig.15

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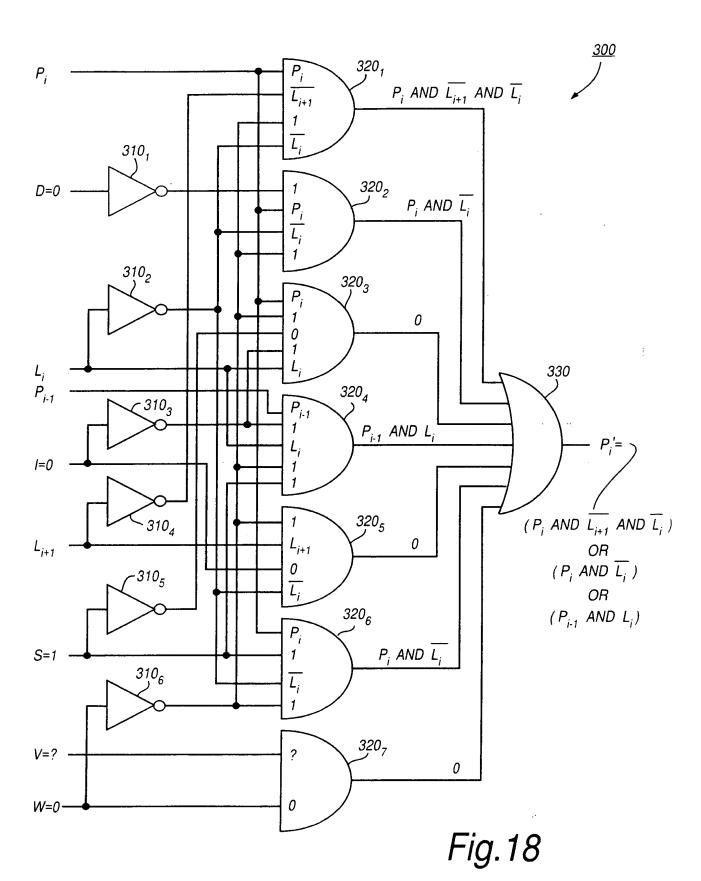Ref. No. 0808.65566
Sheet 15 of 18   (312) 360 0080

15/18

Fig.16

16/18

Fig.17

17/18

Fig.18

PREDICATED EXECUTION OF INSTRUCTIONS . . .
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Ref. No. 0808.65566
Sheet 18 of 18   (312) 360 0080

18/18

Fig.19